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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/936,041	12/18/2001	Ichio Yudasaka	110553	7809

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EXAMINER
ROMAN, ANGEL

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 04/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/936,041	Applicant(s) YUDASAKA ET AL.	
	Examiner Angel Roman	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

2. Claims 2 and 7-13 are objected to because of the following informalities: the word --wherein-- should be inserted after the first comma. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily

published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1- 4, 6, 7 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Blake U.S. Patent 4,965,213.

Blake discloses a method of manufacturing a thin-film transistor, comprising; forming a channel region facing a gate electrode through a gate insulating film; forming source and drain regions18 connected to the channel region in a semiconductor film that is formed on a surface of an insulating substrate 4; and forming a recombination center 38 that captures carriers in the channel region by introducing an impurity into said channel region. Introducing said impurity into said channel region is carried out by injecting the impurity from a surface side of said channel region (see figure 5a) after a crystallization process (see column 3, lines 9-17) and after the gate insulating film 14 and the gate electrode 10 are sequentially formed. An average projected range of the impurity in said process of introducing an impurity being from a center in a direction of thickness of said channel region to an interface between the channel region and the gate insulating film (see figure 5c). Said impurity being at least one kind selected from the group including inert gases, metals, Group III elements, Group IV elements and Group V elements (see column 6,lines 45-50).

5. Claims 1-3, 5 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Gardner et al. U.S. Patent 6,005,285.

Gardner et al. discloses a method of manufacturing a thin-film transistor, comprising; forming a channel region facing a gate electrode 30 through a gate insulating film 28; forming source and drain regions 36 connected to the channel region in a semiconductor film 14 that is formed on a surface of an insulating substrate 10; and forming a recombination center 26 that captures carriers in the channel region by introducing an impurity 22, 24 into said channel region. Said impurity being at least one kind selected from the group including inert gases, metals, Group III elements, Group IV elements and Group V elements (see column 8, lines 3-20). The process of introducing said impurity into said channel region is carried out by injecting the impurity from a surface side of said channel region before a process of forming said gate electrode on a surface side of the channel region (see figure 4) and an average projected range of the impurity in said process of introducing an impurity being from a center in a direction of thickness of said channel region to an interface between the channel region and a layer 12 located on said substrate 10.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. U.S. Patent 6,005,285

Gardner et al. is applied as above but lacks anticipation on introducing said impurity to said channel region by impurity diffusion from an impurity diffusion source arranged at a lower layer side of said channel region and performing it during a crystallization process of a semiconductor film so as to form said channel region. Diffusing an impurity by diffusing from an impurity diffusion source arranged at a lower layer side of a channel region during a crystallization process of a semiconductor film is a conventional process in the art, therefore it would have been obvious to one having ordinary skills in the art at the time the invention was made to use a diffusion layer arrange at a lower layer side of a channel region to diffuse an impurity into a channel region during a crystallization process in the primary reference of Gardner et al. since diffusing from a solid layer is a well known method of introducing an impurity into a

layer. Furthermore diffusing an impurity by diffusing from an impurity diffusion source arranged at a lower layer side of a channel region during a crystallization process of a semiconductor film is an alternate method of introducing an impurity and is only considered to be routine optimization of the prior art disclosed by Gardner et al. and a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, manufacturing costs, etc. (see In re Boesch, 205 USPQ 215 (CCPA 1980)), and since neither non-obvious nor unexpected results, i.e., results which are different in kind and not in degree from the results of Gardner et al., will be obtained as long as an impurity is introduce as already suggested by the Gardner et al..

9. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blake U.S. Patent 4,965,213.

Blake is applied as above but lacks anticipation on disclosing a crystallization process being laser annealing and disclosing a temperature below 300°C for following processing of the transistor.

With respect to using laser annealing for the crystallization process, laser annealing is a conventional process used to crystallized amorphous layers, therefore it would have been obvious to a person having ordinary skills in the art at the time the invention was made to use a laser annealing process in the primary reference of Blake since is a known method of performing a crystallization process (see column 3, lines 10-15).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Son discloses a semiconductor device with a damage portion at an interface between an insulator and an active layer. Forbes et al. discloses a transistor comprising a channel region with variable voltage. Burnham et al. and deSouza et al. discloses methods of diffusing impurities from an underlying layer. Yamaguchi et al. discloses a method of making a transistor by using laser annealing as a recrystallizing process (see column 2, lines 34-40).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (703) 306-0207. The examiner can normally be reached on Monday-Friday 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800

AR
March 24, 2002